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<u>L16</u>	L14 and l12	11	<u>L16</u>
<u>L15</u>	L14 and l10	32	<u>L15</u>
<u>L14</u>	L13 and hash\$4	50	<u>L14</u>
<u>L13</u>	(histor\$4 near8 pattern\$1 or strid\$4) and branch\$3 near6 predict\$5	307	<u>L13</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<u>L12</u>	(711/123-221)[CCLS]	21419	<u>L12</u>
<u>L11</u>	(712/215-300)![CCLS]	7144	<u>L11</u>
<u>L10</u>	(712/215-300)[CCLS]	7144	<u>L10</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L9</u>	predict\$4 near8 branch\$3 near8 (histor\$4 or pattern\$1 or strid\$3) near6 shift\$3	37	<u>L9</u>
<u>L8</u>	branch\$3 near8 (histor\$4 or pattern\$1 or strid\$3) near6 shift\$3	194	<u>L8</u>

<u>L7</u>	L5 and shift\$5	1	<u>L7</u>
<u>L6</u>	L5 and shift\$5	1	<u>L6</u>
<u>L5</u>	5996071.pn.	2	<u>L5</u>
<u>L4</u>	L2 and (strid\$3 or pattern\$1)	7	<u>L4</u>
<u>L3</u>	L2 and stird\$3	0	<u>L3</u>
<u>L2</u>	hash\$3 near5 address\$3 near6 predict\$5	31	<u>L2</u>
<i>DB=USPT; PLUR=YES; OP=OR</i>			
<u>L1</u>	5996071.pn. and hash\$5	0	<u>L1</u>

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Citation



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» Key

IEEE JNL IEEE Journal or Magazine

IEEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

[view selected items](#)[Select All](#) [Deselect All](#)**1. Thread partitioning and value prediction for exploiting speculative thread-level parallelism**

Marcuello, P.; Gonzalez, A.; Tubella, J.;

[Computers, IEEE Transactions on](#)

Volume 53, Issue 2, Feb 2004 Page(s):114 - 125

Digital Object Identifier 10.1109/TC.2004.1261823

[AbstractPlus](#) | Full Text: [PDF](#)(2143 KB) IEEE JNL[Rights and Permissions](#)**2. Branch prediction using both global and local branch history information**

Chang, M.-C.; Chou, Y.-W.;

[Computers and Digital Techniques, IEE Proceedings-](#)

Volume 149, Issue 2, March 2002 Page(s):33 - 38

Digital Object Identifier 10.1049/ip-cdt:20020273

[AbstractPlus](#) | Full Text: [PDF](#)(594 KB) IEEE JNL**3. Fast Configuration of an Energy-Efficient Branch Predictor**

Hallschmid, P.; Saleh, R.;

[Emerging VLSI Technologies and Architectures, 2006. IEEE Computer Society Annual Symposium](#)

Volume 00, 02-03 March 2006 Page(s):289 - 294

Digital Object Identifier 10.1109/ISVLSI.2006.44

[AbstractPlus](#) | Full Text: [PDF](#)(312 KB) IEEE CNF[Rights and Permissions](#)**4. Exploring design space of scalable per-address branch predictors**

Kongmunvattana, A.; Tiamkaew, E.;

[TENCON 2004, 2004 IEEE Region 10 Conference](#)

Volume B, 21-24 Nov. 2004 Page(s):156 - 159 Vol. 2

Digital Object Identifier 10.1109/TENCON.2004.1414555

[AbstractPlus](#) | Full Text: [PDF](#)(1848 KB) IEEE CNF[Rights and Permissions](#)**5. Value predictors for reuse through speculation on traces**

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



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27-29 Oct. 2004 Page(s):48 - 55

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-  **6. Fast path-based neural branch prediction**  
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-  **7. Cost-effective graceful degradation in speculative processor subsystems: the branch predic**  
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